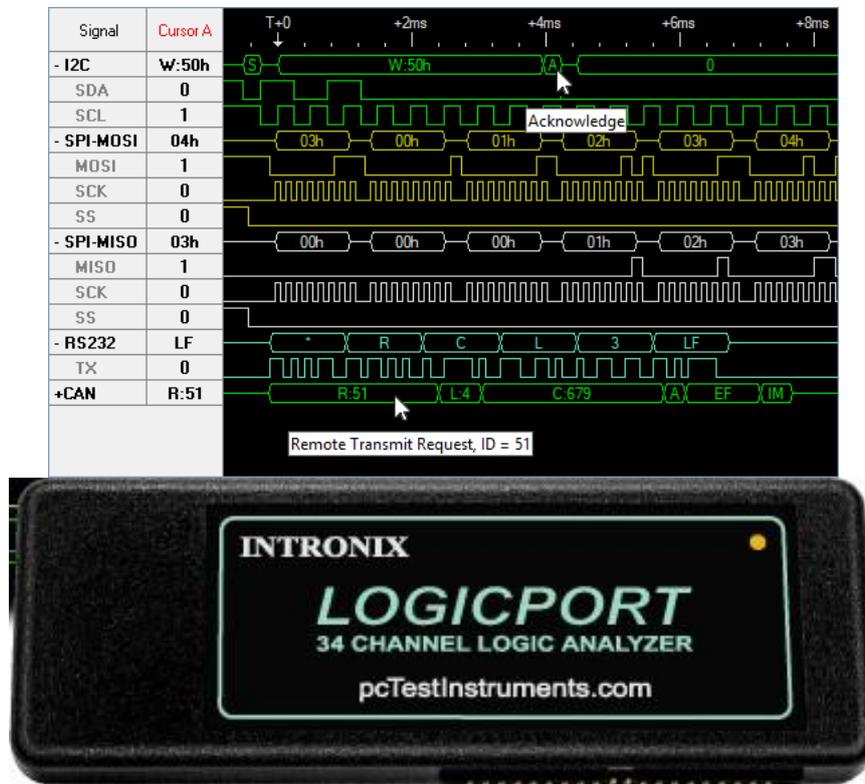




34 CHANNEL LA1034 LOGICPORT LOGIC ANALYZER



- ▶ 500MHz Timing-Mode (Internal Clock)
- ▶ 200MHz State-Mode (External Clock)
- ▶ Advanced Multi-Level Triggering
- ▶ Real-Time Sample Compression
- ▶ +6V to -6V Adjustable Logic Threshold
- ▶ CAN, I2C, SPI, RS232, 1-Wire and more
- ▶ Built-in 300MHz Frequency Counter
- ▶ USB 1.1, 2.0, 3.0 Compatible

The LA1034 LogicPort logic analyzer fills the void between expensive analyzers with many channels, and inexpensive analyzers with few channels and limited sample rates.

The LogicPort provides 34 channels sampled at 500MHz. This includes two state-clock inputs which function as normal sampled channels in timing-mode. The LogicPort logic analyzer's hardware is controlled and powered via your PC's USB 2.0 port for the ultimate in convenience and portability.

Features include multi-level sequential trigger capability, qualified state-mode sampling with adjustable setup/hold window, selectable logic sense and threshold, built-in interpreters for CAN, I2C, SPI, 1-wire, RS232 and ISO7816-3 (SIM/Smart Card) protocols and much more.

The LogicPort's advanced trigger features allow it to trigger on simple or complex sequences of edges, patterns and bus numerical ranges, as well as on specified pattern, range or pulse durations.

You'll find the LogicPort to be feature-rich, yet simple to use. The installation includes real-world examples of actual acquired data. Explore a 125MHz SDRAM interface sampled at 500MHz, the outputs of a 100MHz A/D converter sampled in state mode, interpreted CAN, I2C, SPI, 1-Wire, SIM and RS232 data streams, activity on a typical Intel processor bus and more.



Sampled channels: 34

Timing mode sample rate: 1KHz to 500MHz (uses internal clock)

State mode sample rate: 0 to 200MHz (clock provided by circuit under test)

Sample buffer: 34 x 2048 samples

Maximum sample compression: 2³³ to 1 (sample rates to 200MHz)

Trigger sequencer: 250MHz max, 4ns minimum pulse width

Trigger capability:

Edges - Rising, Falling, Either (multiple channels, any combination)

Patterns - True, False, Entered, Exited (across any / all channels)

Bus Value - Equal, Not Equal, Less Than, Greater Than, In Range, Not in Range

Occurrence Count - Range of 1 to 1,048,576 Consecutive or Cumulative

Duration - Equal, Less Than, Greater Than, Within Range (samples or time)

Input impedance: 200K Ohms, paralleled by <5pF

Frequency counter range: 300MHz with 10Hz resolution, 4 channels

Threshold range: adjustable +6 to -6 volts with 50mv resolution

Threshold accuracy: +/- (100mV + 5% of setting)

Channel to channel skew: 0.6ns typical, 1.0ns max

State mode Setup/Hold times: 2.0/0ns, window adjustable +/-2.5ns

Input sensitivity: 0.25Vpp @50MHz, 0.5Vpp @150MHz, 0.8Vpp @250MHz

Input dynamic range: 10 volts peak-peak

Maximum input: +/-40 volts DC, 15 volts peak-peak pulse amplitude

Timebase accuracy: +/-0.005% over full temperature range

Input Probe: Teflon insulated leads terminated with female contacts compatible with 0.025"-0.030" round or square pins.

Power supply current: 200 milliamps max (supplied by USB)

Temperature range: operating +5 to +50C, storage -10 to +65C

Interpreted Protocols (included):

Asynchronous Serial (RS232, RS422 and RS485 to 25Mbps)

Synchronous Serial (SPI, PS2 and proprietary formats)

Inter-Integrated-Circuit (I2C)

CAN 2.0A and 2.0B

Synchronous Parallel (Quad/multi-IO SPI and proprietary formats)

1-Wire (Dallas/Maxim devices/iButton)

ISO7816-3 (Smart Card and SIM devices)

Minimum system requirements:

Intel Pentium 4 or AMD Athlon (1.6GHz or faster recommended)

32MB available memory (128MB recommended)

800 x 600 standard DPI display (1920 x 1080 recommended)

USB 1.1, 2.0 or 3.0 port

The LA1034 is compatible with the following operating systems:

Windows XP (32 and 64 bit versions)

Windows Vista (32 and 64 bit versions)

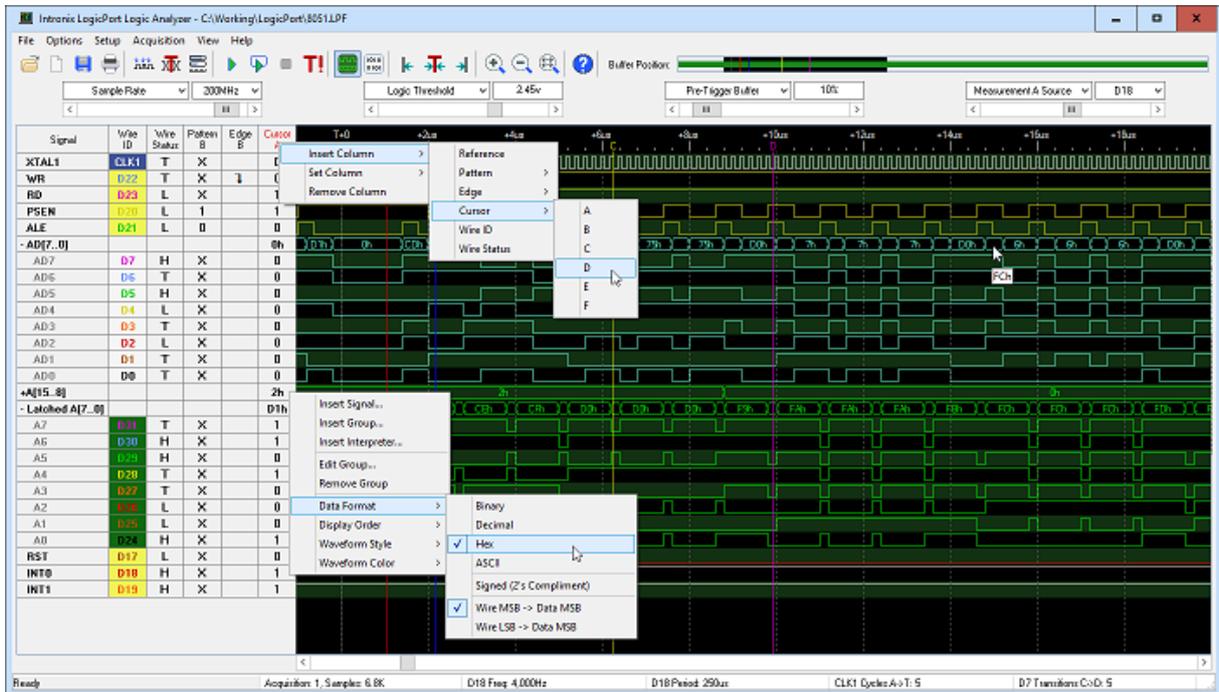
Windows 7 (32 and 64 bit versions)

Windows 8 (32 and 64 bit versions except ARM-based)

Windows 10 (32 and 64 bit versions except ARM-based)



LogicPort Waveforms

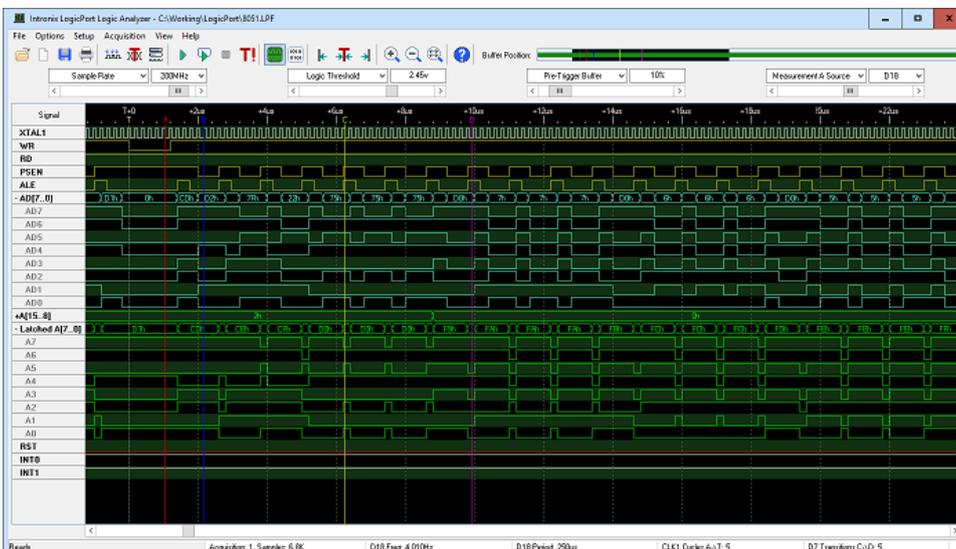


The LogicPort's user interface has been designed for maximum data viewing area. This is one of the major advantages of PC-based test instruments over conventional stand-alone test equipment.

This image shows a few of the 10 different columns which can be included in the waveform display. Trigger patterns and edges are specified by clicking appropriate cells in the table. Colors in the Wire ID column match the color-coded probe supplied with the LogicPort. A Wire Status column is available to show the real-time status of inputs regardless of sample mode or rate. With a couple of mouse clicks you can temporarily hide the columns to get a full-screen view of the acquired data as shown below.

Groups of signals can be shown as composite waveforms with data annotated in a selectable format. A group of digital signals can also be shown as a signed or unsigned *analog* waveform. The open menu shows some of the data formatting options available. This menu was opened by right-clicking on a group in the waveform table. The software includes numerous context-sensitive menus providing convenient access to commonly used features.

Interpreter are included for several common protocols. Transactions using these protocols can be translated, and the resulting high-level data displayed along with the acquired waveforms.





LogicPort State List

The screenshot shows the Intronix LogicPort Logic Analyzer interface. The main window displays a state list table with columns for signals and their values over time. A 'Project Notes' dialog box is open, providing context for the data. A context menu is also visible, showing options for cursor placement and scrolling.

| Relative to Reference | XTAL1 | WR | RD | PSEN | ALE | AD[7..0] | A[15..8] | Latched A[7..0] | RST | INT0 | INT1 |
|-----------------------|-------|----|----|------|-----|----------|----------|-----------------|-----|------|------|
| -1.590ns | 1 | 1 | 1 | 1 | 1 | D1h | 03h | D3h | 0 | 1 | 1 |
| -1.560ns | 1 | 1 | 1 | 1 | 1 | D1h | 03h | D1h | | | |
| -1.530ns | 0 | 1 | 1 | 1 | 1 | D1h | 03h | D1h | | | |
| -1.400ns | 1 | 1 | 1 | 1 | 1 | D1h | 03h | D1h | | | |
| -1.390ns | 1 | 1 | 1 | 1 | 0 | D1h | 03h | D1h | | | |
| -1.320ns | 0 | 1 | 1 | 1 | 0 | D1h | 03h | D1h | | | |
| -1.200ns | 1 | 1 | 1 | 1 | 0 | D1h | 03h | D1h | | | |
| -1.120ns | 0 | 1 | 1 | 1 | 0 | D1h | 03h | D1h | | | |
| -1.000ns | 1 | 1 | 1 | 1 | 0 | D1h | 03h | D1h | | | |
| -880ns | 1 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -920ns | 0 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -800ns | 1 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -780ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -720ns | 0 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -600ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -520ns | 0 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -400ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -320ns | 0 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -200ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| -120ns | 0 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| T+780ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +80ns | 0 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +200ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +280ns | 0 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +400ns | 1 | 0 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +430ns | 1 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +490ns | 0 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +600ns | 1 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +620ns | 1 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +630ns | 1 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +640ns | 1 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +680ns | 0 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +800ns | 1 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +880ns | 0 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +1,000ns | 1 | 1 | 1 | 1 | 1 | 00h | 03h | D1h | | | |
| +1,010ns | 1 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +1,080ns | 0 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +1,200ns | 1 | 1 | 1 | 1 | 0 | 00h | 03h | D1h | | | |
| +1,220ns | 1 | 1 | 1 | 0 | 0 | 00h | 03h | D1h | | | |
| +1,230ns | 1 | 1 | 1 | 0 | 0 | 00h | 03h | D1h | | | |
| +1,240ns | 1 | 1 | 1 | 0 | 0 | 02h | 03h | D1h | | | |

Project Notes:

This example shows activity on the bus of an Intel 8051 series microcontroller. The 8051 multiplexes its data and the lower 8 bits of its address on the bus. The signals in group "AD[7..0]" are sampled from these pins on the 8051.

The circuit under test uses an external TTL latch to capture the low address when ALE from the controller is high. The signals in group "Latched A[7..0]" are sampled from the outputs of this latch.

When the 8051 sets PSEN high, it is accessing data memory. When the 8051 is accessing program memory, PSEN is low.

With this information, we can observe the following memory cycles:

- At cursor A the 8051 writes the value 0h to data memory address 20h.
- At cursor B the 8051 reads the value D2h from program memory address 20h.

You can see these memory cycles in the state list tab as well. Note that the state list tab shows the state of the bus at the time of the memory cycle.

The LogicPort's state list displays data in tabular form. The data can be shown in a "condensed" form, showing only unique states along with a time stamp. Columns can be rearranged as desired, and the data format can be specified separately for each column. The open menu shows a few of the functions available with a right-click of the mouse. At the bottom of the window, up to four chosen measurements can be displayed.

Measurements can range from the interval or transition count between cursors, to a frequency or period measured by the LogicPort's built-in frequency counter. This real-time counter is active regardless of sample mode or rate and can measure frequencies up to 300MHz with 10Hz resolution. The counter will measure and display as many as four channels at a time.

In the upper right corner of the window you can see the buffer position indicator. This indicator shows the relative positions of the cursors and displayed data within the sample buffer.



LogicPort Trigger Setup

Trigger Setup

Trigger: When level A is satisfied and then level B is satisfied Prequalify Pattern/Value Terms

Level A conditions:

- Edge A occurs time(s) Cumulative
- Pattern A is True and
- Value of AD[7..0] is In range to
- For duration In range to Seconds

Level B conditions:

- Edge B occurs time(s) Consecutive while
- Pattern B is False and
- Value of A[15..8] is Equal to
- For duration Less than Samples

Plain-English trigger setup makes the LogicPort easy to use. Trigger schemes can be as simple or complex as required. The image above shows a fairly elaborate scheme, while the image below shows one of the simplest possible schemes. Patterns and edges are specified in the waveform window.

Trigger Setup

Trigger: When level A is satisfied Prequalify Pattern/Value Terms

Level A conditions:

- Edge A occurs time(s)
- Pattern A is True
- Value of AD[7..0] is Equal to
- For duration Greater than Seconds

Level B conditions:

- Edge B occurs time(s)
- Pattern B is False
- Value of A[15..8] is Equal to
- For duration Less than Seconds



LogicPort Sample Mode Setup

In timing mode, the LogicPort acquires samples using its internally generated sample clock. The user can select a desired rate from 1KHz to 500MHz for this internal clock.

In state mode, the LogicPort samples on the specified edge of an external clock supplied by the hardware under test. The LogicPort's Setup/Hold window is adjustable relative to the clock input, a feature usually found only on much more expensive units. The adjustable window provides greater flexibility when sampling high-speed signals with tight timing margins. Notice that in this particular example the sample window has been adjusted to a position 2.5ns *before* the rising edge of the external clock. Qualified sampling has also been enabled, causing the LogicPort to sample *only* when CLK2 is low. Qualified state mode sampling is useful for de-multiplexing processor buses which multiplex Address and Data information onto the same bus. It can also be used to capture data directed toward a particular peripheral by using the peripheral's enable signal as a qualifier.

Sample compression is available for both timing mode and state mode. When compression is enabled, Pre-Fill and Post-Fill time limits allow you to specify how long you are willing to wait for an acquisition to complete. This is useful when the hardware under test has few transitions or has intermittent bursts of activity. In these situations the sample compression ratio can be extremely high, and it could take a long time to complete an acquisition. Under certain circumstances the LogicPort can pack *hours* of data into its sample buffer.

Sample Mode Setup

Timing Mode (Internal Sample Clock)

State Mode (External Sample Clock)

Sample data 2.5ns before the Rising edge of CLK1

Sample only when qualifier CLK2 is

Base time scale on a clock of Hz

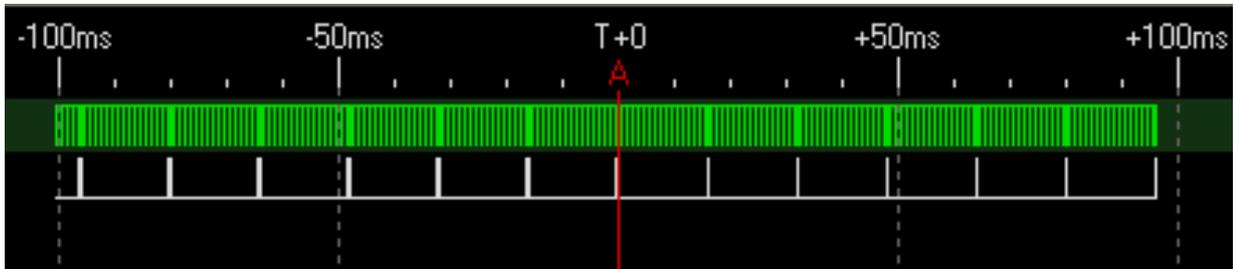
Enable Compression

Pre-Fill Time Limit: Post-Fill Time Limit:

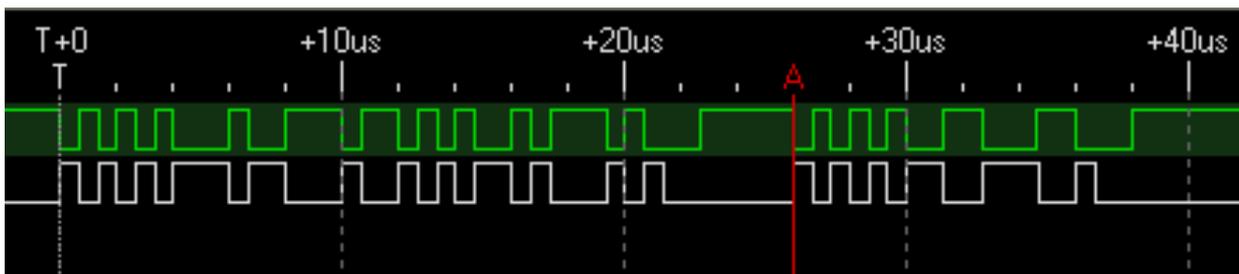


LogicPort Sample Compression

The LogicPort's real-time hardware sample compression or "transitional sampling" allows it to pack much more data into its sample buffer. Since memory is only written when signals change, the time between signal transitions is essentially "free".



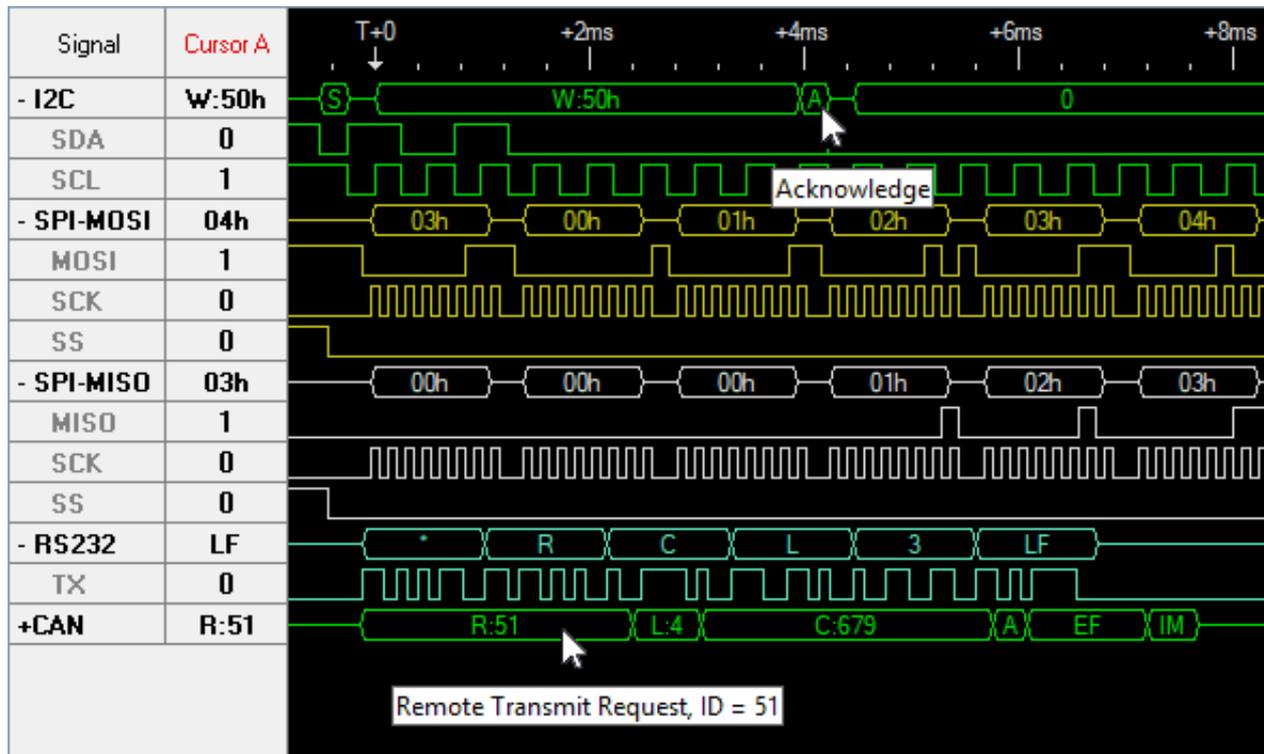
The trace above shows the LogicPort capturing close to 10 megasamples (MSa) of data while sampling at 50MHz over a period of nearly 200ms. The trace below shows a very small portion of that same captured data with the time scale reduced (zoomed in) by a factor of 5000.



You won't always capture this much data, but you'll notice that compression tends to work best right when you need it the most. Specifically, it is most effective when you need to capture events separated by significant time intervals while maintaining high resolution.



LogicPort Interpreters



The LogicPort's software includes interpreters for CAN, I2C, Synchronous Serial (SPI), Asynchronous Serial (RS232), Dallas 1-Wire (iButton), Quad/multi-IO SPI and ISO7816-3 (SIM and Smart Card) protocols. Its Synchronous Serial interpreter is very flexible and interprets 3-Wire, Microwire, PS/2 and other proprietary protocols in addition to SPI. The interpreted high-level data can be displayed along with the acquired waveforms as shown above, or in tabular form as shown below.

Interpreted values can be displayed in Binary, Decimal, Hex or ASCII format. Mnemonics are used to allow more data to be displayed within the available area. "Data tips" show expanded information when the mouse cursor is hovered over a mnemonic. In this example, the I2C "Acknowledge" bit is represented by the mnemonic "A".

As you can see, the LogicPort is capable of simultaneously interpreting multiple protocols. In fact, using its 34 channels the LogicPort can simultaneously capture and interpret any combination of up to 17 separate I2C interfaces, 8 SPI ports, 34 CAN or RS232 data streams.

| Relative to Trigger | I2C | SPI-MOSI | SPI-MISO | RS232 | CAN |
|---------------------|-------|----------|----------|-------|-------|
| T-502,970ns | S | | | | |
| 0ns | W:50h | 03h | 00h | * | R:51 |
| +3,975,690ns | A | 00h | 00h | R | L:4 |
| +4,474,650ns | 0 | 01h | 00h | C | C:679 |
| +8,450,340ns | A | 02h | 01h | L | A |
| +13,107,210ns | Sr | 03h | 02h | 1 | EF |
| +13,610,050ns | R:50h | 04h | 03h | LF | IM |
| +17,585,740ns | A | 05h | 04h | * | |
| +18,088,580ns | 0 | | | R | |
| +22,064,270ns | A | | | C | |
| +22,563,350ns | 1 | | | L | |
| +26,539,040ns | A | | | 2 | |
| +27,038,120ns | 2 | | | LF | |
| +31,013,810ns | A | | | * | |
| +31,512,840ns | 3 | | | R | |
| +35,488,520ns | A | | | C | |
| +35,987,610ns | 4 | | | L | |
| +39,963,290ns | N | | | 3 | |
| +40,716,300ns | P | | | LF | |